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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,432	02/06/2004	Toshiki Kaneko	501.43456X00	6107

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,432	KANEKO ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on January 11, 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 4-8, 13, and 14 are rejected under 35 U.S.C. 102(a) as being anticipated by Ohtani et al. (US 6,545,359 B1).

In re claims 1 and 7, Ohtani et al. shows (figs. 1A-1D) a display device having thin film transistors on a substrate (101) thereof, wherein the display device includes gate patterns (106) in each of which a gate line (1') and a gate electrode (105) of the thin film transistor are integrally formed, and drain lines (113); an insulation film (111) covers the gate pattern; the gate pattern is constituted by at least three-layered films consisting of a lowermost layer (105a), an intermediate layer (105b) formed of at least one layer and an uppermost layer (105c) at least at either a portion of the thin film transistor or a portion of the gate pattern which crosses a drain line, the intermediate layer is formed of a material selected from the group consisting of pure Al, an Al alloy, pure Ag, an Ag alloy, pure Cu and a Cu alloy (col. 15, lines 15-51), and the uppermost layer and the lowermost layer are formed of a metal (Ta) having a melting point higher than the melting point of the material (Al) of the intermediate layer. End portions of the

intermediate layer (105b) are recessed from end portions of the uppermost layer and end portions of the lowermost layer.

In re the rest of the limitations of claim 7, Ohtani shows (figs. 18A-18C) alternate embodiments of the gate electrode in which end portions of the uppermost layer (15) are spaced inwardly from end portions of the lowermost layer (13), and at the same time, end portions of the intermediate layer (14) are recessed from end portions of the uppermost layer and end portions of the lowermost layer.

In re claim 4, Ohtani shows (figs. 18A-18C) alternate embodiments of the gate electrode in which end portions of the uppermost layer (15) are spaced inwardly from end portions of the lowermost layer (13).

In re claim 5, 6, 8, and 14, Ohtani shows (figs. 1A-1D) the thin film transistor including a semiconductor layer (104 or 100) and the gate electrode 9105 or 106) is arranged above the semiconductor layer. Ohtani does not specifically disclose that the layer includes a polycrystalline semiconductor but is a crystalline semiconductor layer. However, polycrystalline is a type of crystalline semiconductor layer.

In re claim 13, Ohtani shows (figs. 1A-1D) that the semiconductor layer includes an LDD region (108) and the lowermost layer of the gate electrode has at least a portion that is overlapped by the LDD region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (US 6,545,359 B1) as applied to claims 1, 7, and 8 above, and further in view of Jeong et al. (US 6,081,308)

In re claims 2, 3, 9, and 10, Ohtani shows all of the elements of the claims except the specific materials of the uppermost and lowermost layers being of pure Mo, Mo alloy, or Mo-W. Jeong et al. discloses (col. 9, lines 57-67) a multi-layered gate line for an LCD that uses a Mo-W alloy for the upper layer. The Mo-W alloy prevents hillock formation in the Al layer and reduces the number of lithography steps (col. 12, lines 52-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the uppermost and lowermost layers of the gate electrode of Ohtani by using Mo-W as taught by Jeong to prevent hillock formation in the Al intermediate layer and reduce the processing steps.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (US 6,545,359 B1) as applied to claims 7 and 8 above and further in view of Watanabe et al. (US 6,255,706 B1).

In re claims 11 and 12, Ohtani shows all of the elements of the claims except the etching properties of the uppermost layer and the lowermost layer and those layers being Mo-W and Mo-Cr. Watanabe discloses (col. 3, lines 37-57) that a gate electrode having a laminated structure comprises an upper and lower layer having an allow

selected from combinations of Mo, W, and Cr in which the upper layer is different from the lower layer. If Watanabe were to select the alloy of Mo-W as the upper layer and Mo-Cr as the lower layer, then inherently the etching rate of uppermost layer would be fast than the etching rate of the lowermost layer since the materials and structure are the same as the instant invention. With this configuration, the gate forms a tapered shape (as shown in figure 4) and has a highly reliable structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the materials of the gate electrode of Ohtani by using the desired materials of Watanabe to form a tapered gate having a reliable structure.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kakuda et al. (US 5,162,933) discloses a laminated gate structure having various Mo alloys and the benefits of using such materials.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
March 29, 2006

SPE Kenneth Parker
TC2800